Proton Tests of the Power PC750 Microprocessor

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- **Overview of the Power PC750 Architecture**
- **General Testing Difficulties**
- **Register Testing**
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- **Remote Exploration and Experimentation (RE&E)**
  - Charged with building a super computer (or supercomputer abilities) for space
    - Requires Many Processors
    - Requires Latest and Greatest Devices
  - Intend to use modeling to imitate radiation fault injection
    - Need accurate SEU rates
  - Expected to be used in missions of varying orbit parameters
  - Must keep current
    - PPC 750 will fade as faster processors are embraced in the commercial market
    - Pushing the need for test methods and methodology, not test results (directly)
- **Low Temperature Microgravity Physics Facility (LTMPF) Mission**
  - LTMPF is designated as a test bed for physics experiments
  - Multiple experiments designed for the microgravity environment will fly
  - This is a Space Station mission
    - Will fly in low Earth orbit
    - Will swap between two "facilities"
      - Allows retooling for another experiment
      - Acts as something like redundancy
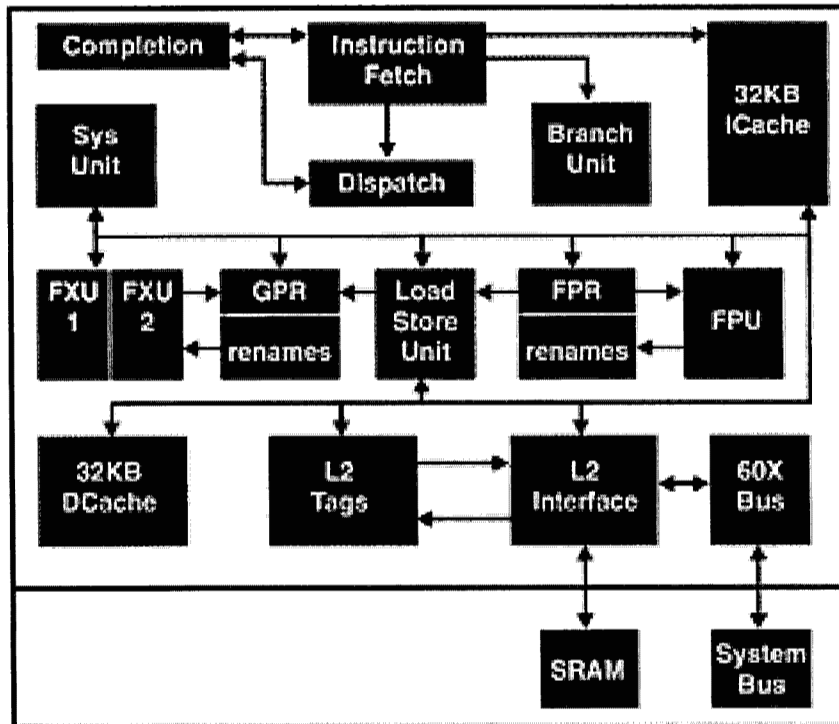
- **Each independent block may have upset problems**
  - Registers
  - Branching Unit
  - Integer Units
  - Floating Point Units
  - MMUs
  - L2 Controller
  - Instruction Unit
  - Load/Store Unit
- **In addtion to these there are other sources**
  - Pipelining difficulties
 - Exception Handling
 - General Lock-up conditions

- **3 - Instructions per Clock, Superscalar RISC architecture**
- **Up to 400 MHz (.25μm process; 266 MHz for .29 *Motorola Features)**
- **32 bit address / 64 bit data buses**
- **L1 Cache**
  - 32K Data
  - 32K Instruction
- **MIPS**
  - 488 at 266MHz
  - 733 at 400MHz
- **Manufacturers**
  - Motorola
  - IBM
  - Thomson

- **The Package Layout of the Power PC 750 Microprocessor forced proton testing**
  - Ball Grid Array
  - Flip Chip
  - Requires rages of > 200μm to reach
- **Test Hardware**
  - Complexity forced board-level testing
  - LTMPF Testing done as board-level also
- **Latchup Monitoring**
  - ATX Power Supply Imitation
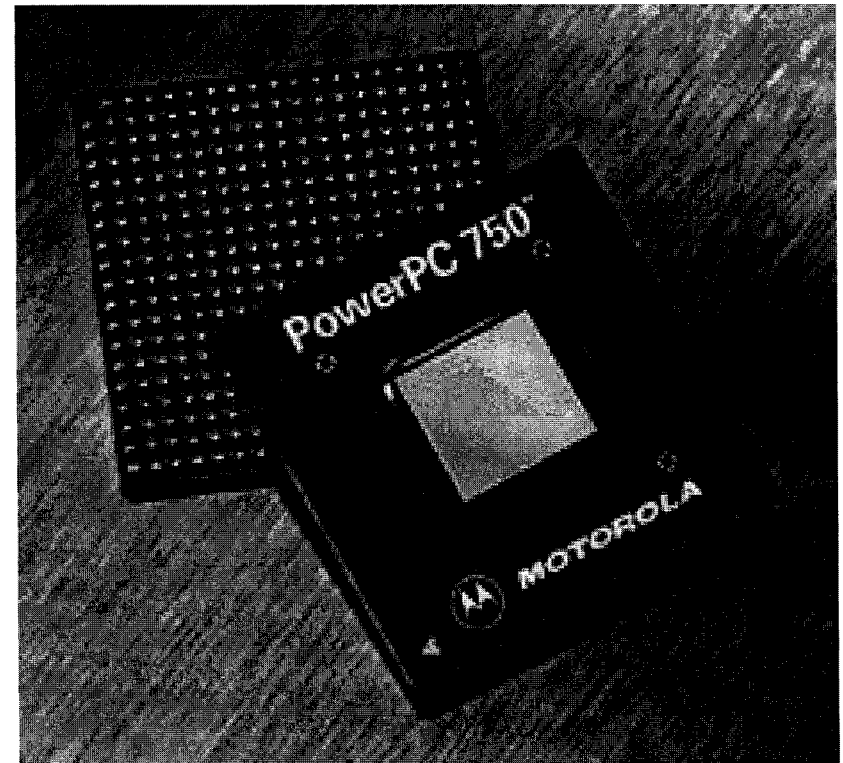
- **Addressed Items in REE Testing (To Date)**
  - Proton Latchup - Addressed with ATX power supply imitation
  - Register Upsets
- **Test Hardware**
  - Motorola's Yellowknife X4 Evaluation Board
- **Test Flow**
  - Setup the test board with known register values, and in known state
  - Run a simple branch loop with no control code
  - Irradiate the device
  - Break out with an external interrupt
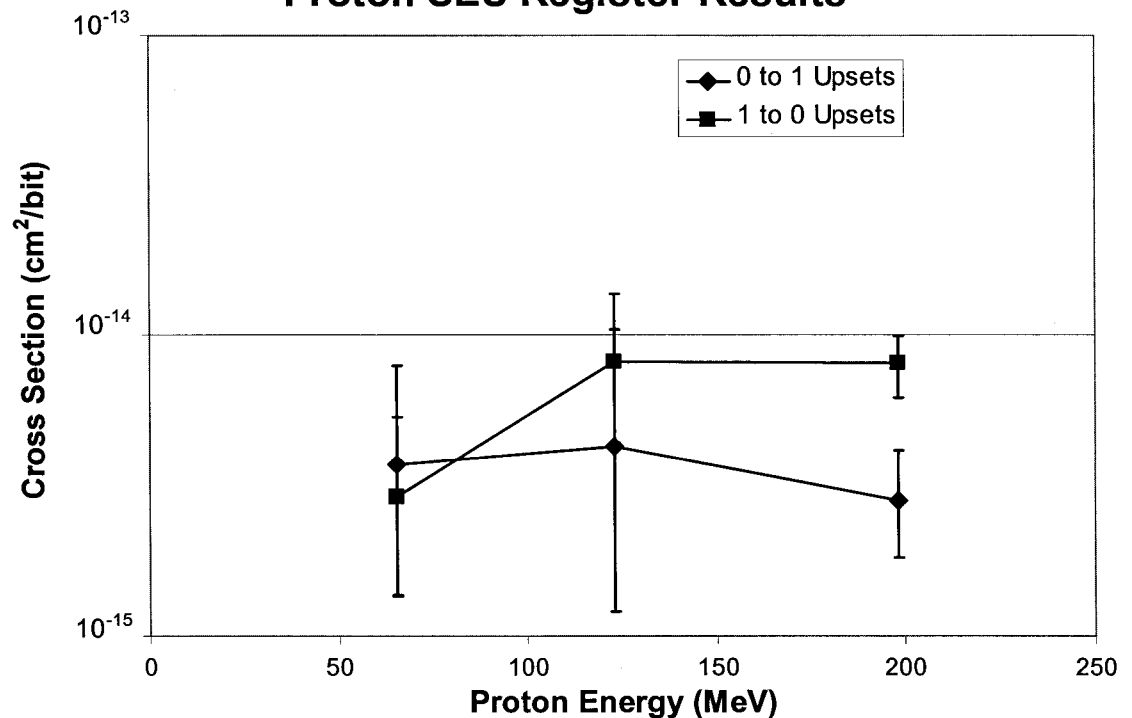 - Check the state of the registers and record any changes

REMOTE EXPLORATION and EXPERIMENTATION PROJECT
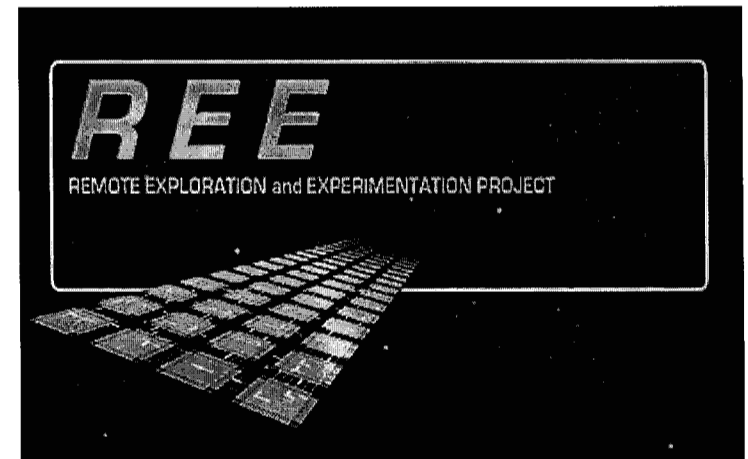
- **General Results**
  - ◆ Cross Section is fairly low - but
  - ◆ Results Confounded by single-event lockups
    - ■ Coarse statistics

- **Specific Results**
  - ◆ Cross Section differs for 0 to 1 and 1 to 0 errors
  - ◆ Evidence cannot show a difference in GPR and FPR rates

Proton SEU Register Results

Legend: 0 to 1 Upsets (◆), 1 to 0 Upsets (■)

X-axis: Proton Energy (MeV)
Y-axis: Cross Section (cm²/bit)
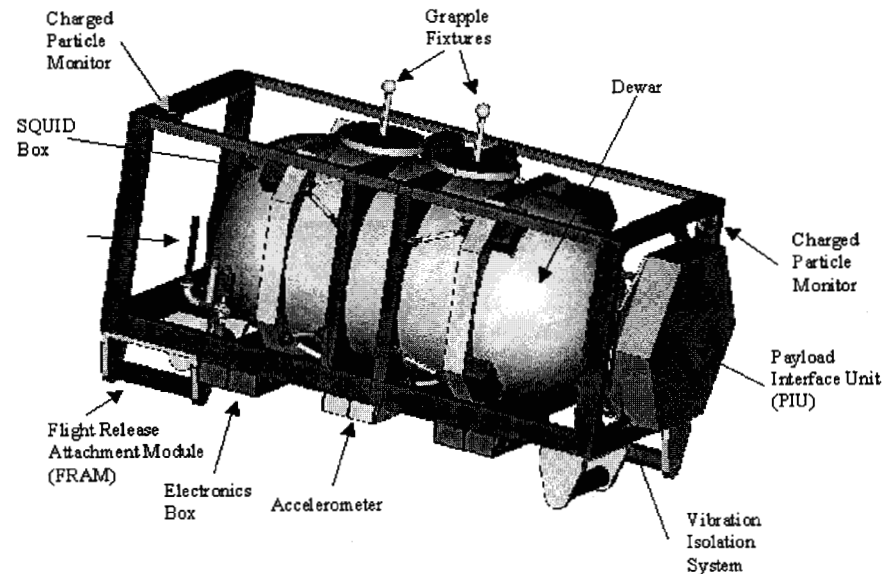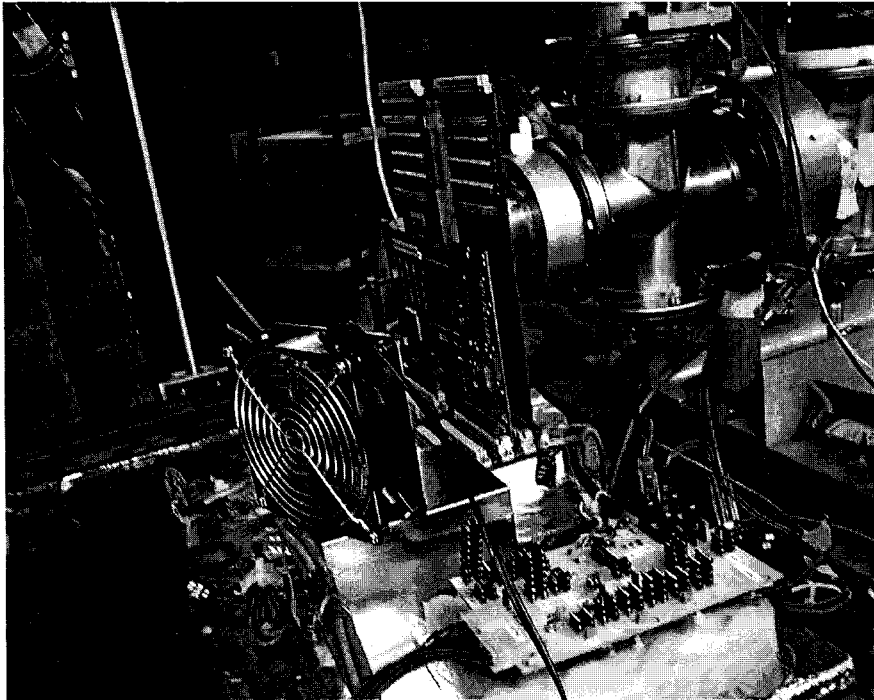
JPL   **NASA**

- **Test Boards**
  - ◆ Several were provided for testing at IUCF
  - ◆ Included VME processor board - primary test vehicle
  - ◆ Also included Yellowknife board and PPC750 with on chip L2 cache

- **Test Programs**
  - ◆ Most test program details are unknown to us
  - ◆ Processor Test
  - ◆ L1 Cache Test
  - ◆ L2 Cache Test
  - ◆ Included many other components

Labels: Charged Particle Monitor, Grapple Fixtures, Dewar, SQUID Box, Charged Particle Monitor, Payload Interface Unit (PIU), Flight Release Attachment Module (FRAM), Electronics Box, Accelerometer, Vibration Isolation System

Low Temperature Microgravity Physics Facility - External Space Station Component

- **Proton test results of the test types:**

SEU Type	Upset Rate
Processor	?/day
L1 Cache bits	?/day
L2 Cache bits	?/day

(will fill in the ?'s)

- **LTMPF Testing was difficult because of on-board resources**
  - Processor
  - Bridge Chip
  - Memory
  - Boot Rom/Flash

- **LTMPF testing is helpful for the RE&E goal - allowing comparison of different testing methods**
- **Additional test capabilities to be developed for RE&E's PPC750 objective**
  - ◆ L1 Cache
  - ◆ Memory Management Units
  - ◆ Additional Special Function Registers
  - ◆ Exception Handling
- **Heavy Ion testing most likely at Texas A&M in June**
  - ◆ Lockheed Martin will provide thinned die (200, 100, and 50μm thick)
  - ◆ Testing will also be done with long range lighter ions at Brookhaven National Laboratory
- **More Realistic Test Situations**
  - ◆ There is a need to do real application testing
  - ◆ Plan is to do testing of application-like software packages under real operating systems.

- **Testing Complications**
  - ◆ Inexact Board-Level testing
  - ◆ Custom Assembly-Level Software
  - ◆ Processor Complexity is difficult to understand
- **Test Part Logistics**
  - ◆ Parts are both ball grid arrays and flip chips
    - ■ Etching and Re-Packaging are not feasible
  - ◆ Methods planned are not optimum because high energy facilities (needed to get through the back of thinned die) are more expensive
- **Application to the Real Client Software**
  - ◆ Test Results: Detailed Register Upset Information
    - ■ Still difficult to determine on orbit upset rate of actual software
  - ◆ Test Results: Board Level Test Results
    - ■ This sort of testing doesn't identify actual upset type reliably
    - ■ May be impossible to determine actual software response
- **Moderate SEU Susceptibility**
  - ◆ Internal bits have a roughly 2×10^{-7} per day upset rate for low inclination Earth orbit
  - ◆ Given there are about 1 million such registers, this is about one register upset a week